CLAIMS

1. A method for aligning an image to be recorded by a direct image scanner on an upper layer of a printed circuit board with an image recorded on a lower layer thereof, the method comprising:

visually imaging a portion of the image on the lower layer; and

recording a pattern on the upper layer, referenced to coordinates of the visual image of the portion.

2. A method according to claim 1 wherein the portion is an alignment pattern recorded on the lower layer.

3. A method according to claim 2 and including forming an opening in the upper layer through which the alignment pattern is visible.

4. A method according to claim 2 wherein the alignment pattern is visible through the upper layer.

5. A method according to claim 1 wherein recording includes:

providing an object aligned with the image portion; and

recording the pattern on the upper layer, referenced to the object.

6. A method according to claim 5 wherein the object comprises holes formed in the upper layer.

7. A method according to claim 5 and including:

imaging the object; and

determining a position of the object,

wherein the pattern is recorded relative to the determined position.

8. A method according to claim 6 wherein the holes comprise holes that do not pass through the lower layer.

9. A method according to claim 6 wherein the holes are vias.

10. A method according to claim 9 wherein the holes comprise functional vias connecting patterns on the upper and lower layers.

11. A method according to claim 6 wherein the images comprise electrical circuits and wherein the holes are not related to an electrical function of the printed circuit board.

12. A method according to claim 6 wherein the holes pass through the upper and lower layers.

13. A method according to claim 6 wherein the holes form an alignment pattern, referenced with the image on the lower layer.

14. A method according to claim 13 wherein the images comprise electrical circuits and wherein the holes are not related to an electrical function of the images

15. A method according to claim 14 wherein the holes pass through the upper and lower layers.

16. A method for aligning an image to be recorded by a direct image scanner on an upper layer of a printed circuit board substrate with a pattern on a lower layer thereof, the method comprising:

detecting at least one hole provided in the upper layer, said at least one hole being provided in predetermined alignment to said pattern and said at least one hole not passing through said lower layer; and

scanning a pattern on the upper layer in predetermined alignment with said at least one hole.

17. A method for recording an image on an upper layer of a multi-layered printed circuit board substrate, the method comprising:

forming at least one hole in an upper layer of a multi-layered printed circuit board substrate, said at least one hole having a known spatial orientation to a pattern formed on one

layer of the substrate and said substrate having at least two layers of circuitry already formed thereon;

acquiring an image of the at least one hole;

calculating a location of the at least one hole from analysis of the image; and

recording a pattern on the upper layer with reference to said location.

18. The method for recording an image according to claim 17 and wherein forming at least one hole comprises forming at least one hole with a laser micro-machining device.

19. The method for recording an image according to claim 17 and wherein forming at least one hole comprises forming the at least one hole in at least the upper layer and not forming at least one hole in at least another layer of said multi-layered printed circuit board substrate.

20. The method for recording an image according to claim 17 and wherein acquiring an image includes acquiring a digital image of the at least one hole.

21. The method for recording an image according to claim 17 and wherein calculating a location of the at least one hole from analysis of the image comprises calculating a location of the at least one hole in a coordinate system of an image recording system.

22. The method for recording an image according to claim 17 and wherein recording a pattern comprises photosensitizing said upper layer and scanning a pattern onto the upper layer with a laser direct imaging system.

23. The method for recording an image according to claim 17 and wherein recording a pattern comprises photosensitizing said upper layer and imaging a pattern onto the upper layer through a mask.

24. A method according to claim 17 wherein said at least one hole a plurality of holes arranged in a non-periodic hole pattern.

25. A method according to claim 24 wherein holes forming said hole pattern do not pass through at least a layer of said multi-layered printed circuit board substrate.

26. A method according to claim 24 wherein holes forming said hole pattern pass through each layer of said multi-layered printed circuit board substrate.

27. A method of image alignment, comprising:

producing an array of elements arranged in a non-periodic pattern on said image; and

matching said pattern with an identical pattern, such that said image is aligned when the patterns overlay each other,

wherein fewer than 50% of the elements of the alignment pattern in the image overlay the pattern in the identical pattern for any position in which the patterns are not aligned.

28. Apparatus for recording an electrical circuit pattern on an upper layer of a multi-layer printed circuit board substrate, comprising:

an alignment pattern generator generating an alignment pattern that is visible on the upper surface of the multi-layer printed circuit board substrate, said alignment pattern having a known orientation with respect to an electrical circuit pattern formed on one non-upper layer of the substrate, said substrate having at least two layers of circuitry already formed thereon;

an alignment pattern location sensor sensing a location of the alignment pattern; and

an electrical circuit pattern generator recording an electrical circuit pattern on said upper surface in a desired orientation with reference to the alignment pattern.

29. Apparatus for recording an electrical circuit pattern according to claim 28, and wherein said alignment pattern generator is a micro machining device.

30. Apparatus for recording an electrical circuit pattern according to claim 29, and wherein micro machining device is a laser drill.

31. Apparatus for recording an electrical circuit pattern according to claim 28, and wherein said alignment pattern is defined by a plurality of holes in said upper surface.

32. Apparatus for recording an electrical circuit pattern according to claim 31, and wherein said plurality of holes is arranged in a non-periodic pattern.

33. Apparatus for recording an electrical circuit pattern according to claim 29, and wherein said alignment pattern is defined by a plurality of micro-machined holes, and wherein said micro-machined holes do not pass through at least one layer in said multi-layered substrate.

34. Apparatus for recording an electrical circuit pattern according to claim 33, and wherein said plurality of micro-machined holes is arranged in a non-periodic pattern.

35. Apparatus for recording an electrical circuit pattern according to claim 28, and wherein said alignment pattern is defined by a plurality of objects deposited on said upper surface, said objects being arranged in a non-periodic pattern.

36. Apparatus for recording an electrical circuit pattern according to claim 35, and wherein said plurality of objects is a plurality of markings.

37. Apparatus for recording an electrical circuit pattern according to claim 36, and wherein said markings are dimples.

38. Apparatus for recording an electrical circuit pattern according to claim 28, and wherein said an alignment pattern location sensor comprises a digital camera and an image processing circuit operative to acquire an image and compute a location of said alignment pattern.

39. Apparatus for recording an electrical circuit pattern according to claim 38, and wherein said location of said alignment pattern is computed in a coordinate system employed by said electrical circuit pattern generator.

40. Apparatus for recording an electrical circuit pattern according to claim 39, and wherein said upper layer includes a photosensitized surface and said electrical circuit pattern generator is a laser direct imaging scanner selectively recording an electrical circuit pattern on said photosensitized surface.

41. Apparatus for recording an electrical circuit pattern according to claim 39, and wherein said upper layer includes a photosensitized surface and said electrical circuit pattern generator comprises a phototool mask and a light projector projecting light through said phototool mask onto said photosensitized surface to selectively record an electrical circuit pattern thereon.

42. Apparatus for aligning a first electrical circuit pattern to be recorded on an upper layer of a multi-layer printed circuit board substrate to a second electrical circuit pattern formed on a lower layer of the multi-layer printed circuit board substrate, comprising:

an alignment pattern location sensor sensing a location of an alignment pattern located on a multi-layered printed circuit board substrate, said alignment pattern having a known orientation to said second electrical circuit pattern; and

an electrical circuit pattern generator recording an electrical circuit pattern on said upper surface in a desired orientation with reference to the alignment pattern.

43. Apparatus for recording an electrical circuit pattern according to claim 42, and wherein said alignment pattern is disposed along said upper layer.

44. Apparatus for recording an electrical circuit pattern according to claim 43, and wherein said alignment pattern is defined by a plurality of holes in said upper surface.

45. Apparatus for recording an electrical circuit pattern according to claim 44, and wherein said plurality of holes is arranged in a non-periodic pattern.

46. Apparatus for recording an electrical circuit pattern according to claim 44, and wherein said plurality of holes do not pass through said lower layer.

47. Apparatus for recording an electrical circuit pattern according to claim 42, and wherein said alignment pattern is defined by a plurality of holes through said multi-layered printed circuit board substrate.

48. Apparatus for recording an electrical circuit pattern according to claim 47, and wherein said plurality of holes is arranged in a non-periodic pattern.

49. Apparatus for recording an electrical circuit pattern according to claim 42, and wherein said alignment pattern is defined by a plurality of visible objects deposited on said upper surface, said visible objects being arranged in a non-periodic pattern.

50. Apparatus for recording an electrical circuit pattern according to claim 49, and wherein said plurality of visible objects is a plurality of markings.

51. Apparatus for recording an electrical circuit pattern according to claim 50, and wherein said markings are dimples.

52. Apparatus for recording an electrical circuit pattern according to claim 42, and wherein said an alignment pattern location sensor comprises a digital camera and image processing circuitry operative to acquire an image and compute a location of said alignment pattern.

53. Apparatus for recording an electrical circuit pattern according to claim 52, and wherein said location of said alignment pattern is computed in a coordinate system employed by said electrical circuit pattern generator.

54. Apparatus for recording an electrical circuit pattern according to claim 53, and wherein said upper layer includes a photosensitized surface and said electrical circuit pattern generator is a laser direct imaging scanner selectively recording an electrical circuit pattern on said photosensitized surface.

55. Apparatus for recording an electrical circuit pattern according to claim 53, and wherein said upper layer includes a photosensitized surface and said electrical circuit pattern generator comprises a phototool mask and a light projector projecting light through said phototool mask onto said photosensitized surface to selectively record an electrical circuit pattern thereon.